Novel HBT with Reduced Thermal Impedance

Darrell Hill, *Member, IEEE,* Ali Khatibzadeh, *Member, IEEE,*
William Liu, *Member, IEEE,* Tae Kim, and Pertti Ikalainen, *Member, IEEE*

***Abstract*—Heterojunction bipolar transistors have been fabricated using a novel process in which the majority of the front side of the chip is metallized to serve as the groundplane. The completed chip is assembled inverted so that the emitters are next to the heat sink; base and collector are contacted using through-wafer vias and microstrip lines on the back side of the chip. These devices show a 50% reduction in thermal impedance compared to conventionally fabricated devices and have achieved power densities of 10 W/mm of emitter length. Such devices are expected to have substantially lower emitter inductance as well, which may lead to improved gain at higher frequencies.**

I. Introduction

GaAs FIELD EFFECT and bipolar transistors are being developed for a range of microwave power applications. Due to the low thermal conductivity of the substrate, the maximum power output of GaAs-based transistors or MMIC's is frequently limited by high junction temperatures due to self-heating. Various approaches for overcoming this limitation have been demonstrated, including flip-chip bump assembly [1], transferal of the epitaxial layers to low-thermal-resistance substrates [2], and the use of thick plated airbridges for heat spreading [3]. However, flip-chip bump assembly requires alignment to custom packages, while epitaxial transfer involves handling of very thin films and relies on expensive diamond substrates. The airbridge heat-spreading technique has demonstrated the highest power density to date, but has certain drawbacks as well. The use of thick (>20 μm) plated patterns requires special photolithography techniques; also, the heat-spread areas require significant amounts of real estate, so that the chip size required to reach a given power level is not as compact as might be expected considering the high power densities that can be achieved. Finally, as the number of fingers placed under the heat-spread airbridge increases, the thermal impedance and emitter inductance associated with the airbridge become less favorable.

We report preliminary results for low thermal impedance heterojunction bipolar transistors (LTI-HBT's) fabricated by a novel process that reduces the thermal impedance by placing the emitters next to the heat sink; base and collector are contacted from the opposite side of the chip using through-wafer vias. In this process, the thermal impedance is independent of chip thickness so that handling of unusually thin films is not required. Also, while compatible with diamond heat sinks and custom packages, the present approach does not require such techniques and offers reduced thermal impedance even for assembly on conventional metal heat sinks. No special lithography techniques or additional heat-spread areas are required. LTI-HBT's are also expected to have very low emitter inductance. While conventional processes ground one or more emitter fingers through a limited number of vias, the emitters of LTI-HBT devices are connected directly to the microwave groundplane. Our simulations indicate that a typical conventional 1-W HBT device loses 1 dB of gain at 10 GHz and 2 dB at 20 GHz because of negative feedback due to nonzero grounding inductance. Imperfect power scaling due to grounding inductance has been reported for HBT's [5].

Manuscript received April 27, 1995.

The authors are with Texas Instruments Corporate Research and Development, Dallas, TX 75265 USA.

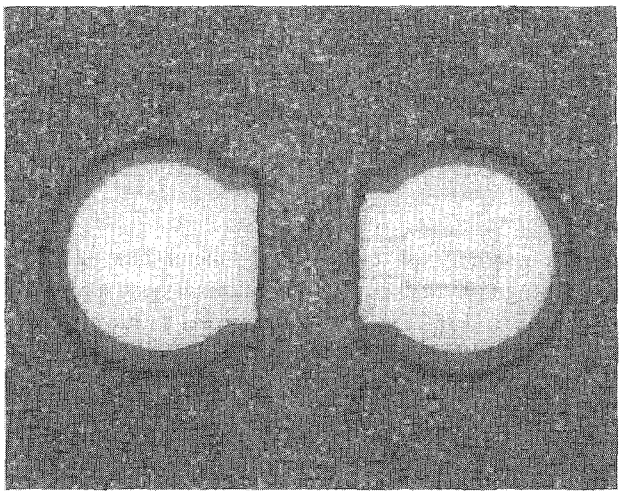
IEEE Log Number 9414645.

II. Device Design and Fabrication

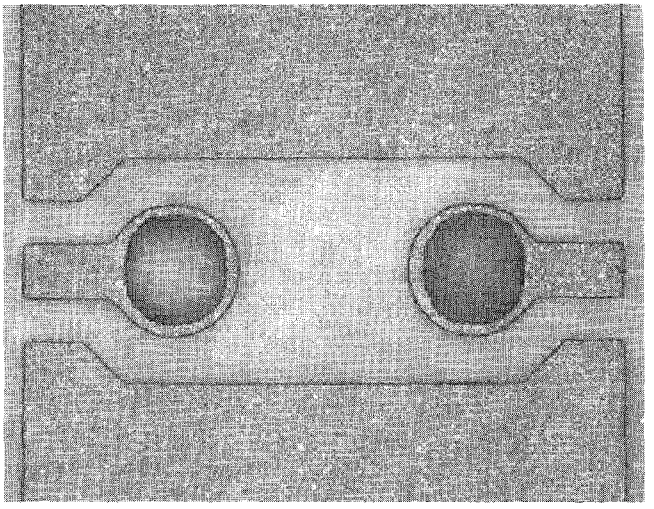
HBT epitaxial structures were grown using metal-organic chemical vapor deposition. The emitter, base, and collector ohmic contacts were defined conventionally using a mesa process. After the contacts were established, most of the frontside surface of the wafer was covered with 3 μm of plated Au, with the exception of metal pads connected to the base and collector contacts. The plated Au was also used to form air-bridges to the emitter contacts. The base and collector pads were then covered with a thick dielectric layer, and an unmasked plating step was performed to increase the total plated Au thickness to approximately 10 μm. The wafer was thinned to 100 μm, and through-wafer vias were etched. Metal was deposited on the backside of the chip and in the vias to form microstrip lines and to contact the base and collector. The wafer was diced, and transistors were assembled with the frontside plated Au attached to a Au pedestal heat sink with Au/Sn solder of approximately 25 μm thickness. The frontside metal thus serves as the groundplane for the microstrip lines that were formed on the backside of the wafer. Because the chip thickness was 10 times greater than the plated metal thickness, no chip bowing was observed. The parasitic capacitance of the base and collector pads to the metallic heat sink is calculated to be significantly smaller than the intrinsic junction capacitances of the HBT device. Fig. 1(a) and (b) shows photographs of the front and back sides of a completed device fabricated using the LTI-HBT process. Fig. 1(c) shows a shematic cross-section of an LTI-HBT attached to a heat sink with Au/Sn solder. The devices had an emitter stripe width of 3.5 μm, with emitter lengths of 30 and 50 μm.

III. Results

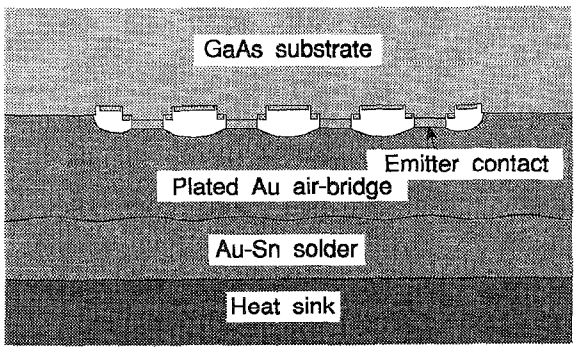
The thermal impedance was measured by determining the temperature coefficient of the base-emitter voltage V_{be} and then monitoring the value of V_{be} as power dissipated in the transistor was increased. Contrary to what was reported in



(a)



(b)



(c)

Fig. 1. Views of completed LTI-HBT device. (a) Front side of chip showing base and collector pads. (b) Back side of chip showing through-wafer vias used to contact base and collector pads. (c) Schematic view of device cross-section and heatsink.

[3], this temperature coefficient is explicitly dependent on the current, decreasing logarithmically with current density [4], as confirmed by our measurements. The temperature coefficient must therefore be determined accurately at the current density used for the thermal impedance measurement.

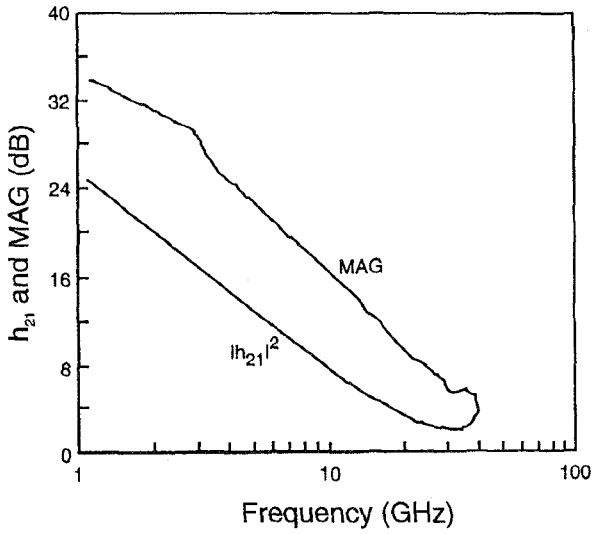


Fig. 2. Small-signal gain characteristics of LTI-HBT with 3.5×30 μm^2 emitter at $V_{CE} = 4$ V, $I_C = 48$ Ma.

The thermal impedance of a device with a 3.5×30 μm^2 emitter was measured to be 410°C/W. The thermal impedance of a conventional, noninverted device is expected to be 890°C based on simulation. Although we have not fabricated a conventional device with exactly these emitter dimensions, we have verified the accuracy of our thermal modeling against direct thermal impedance measurements for a range of device geometries, and we are confident that the 890°C figure is realistic. The LTI approach therefore represents a 50% reduction in thermal impedance compared to the conventional fabrication approach.

LTI-HBT small-signal characteristics were measured from 0.1–40 GHz using on-wafer Cascade probes; as expected, the additional parasitic capacitance was too small to affect device characteristics significantly. Despite the relatively large 3.5×30 μm^2 emitter, the device has good small-signal gain, as shown in Fig. 2. LTI-HBT devices with 3.5×50 μm^2 emitter dimensions were mounted in RF test fixtures and tested under large-signal conditions. At 10 GHz, output power of 500 mW was achieved with 10.5 dB associated gain and 55% power-added efficiency, representing a power density of 10 W/mm of emitter length. This is approximately double the power density expected from a conventionally fabricated device of the same dimensions. The LTI technology is also applicable to multi-finger power HBT's and power amplifiers. Devices with multiple emitter fingers were also tested, but output power densities were typically 25% lower because of an aggressive 10.5 μm pitch (i.e., center-to-center spacing between adjacent emitters was only 10.5 μm). We expect that with a less aggressive pitch, higher power density will be maintained for multifinger HBT's as well.

IV. Summary

We have demonstrated a novel process for fabricating HBT's with reduced thermal impedance by placing the emitters next to the heat sink and contacting the base and collector with through-wafer vias. Devices fabricated with this process have demonstrated 50% lower thermal impedance while main-

taining good microwave power characteristics. A device with a $3.5\times50\ \mu m^2$ emitter achieved 500 mW output power with 10.5 dB associated gain and 55% power-added efficiency at 10 GHz.

ACKNOWLEDGMENT

The authors would like to acknowledge the assistance of T. Session and W. Johnson for device fabrication.

REFERENCES

[1] H. Sato, M. Miyauchi, K. Sakuno, M. Akagi, M. Hasegawa, J. K. Twynam, K. Yamamura, and T. Tomita, "Bump heat sink technology—A novel assembly technology suitable for power HBTs," in *1993 GaAs IC Symp. Dig.*, 1993, pp. 337–340.

[2] G. J. Sullivan, M. K. Szwed, D. A. Hardwick, J. A. Higgins, J. R. Waldrop, and M. F. Chang, "Improved thermal performance of AlGaAs/GaAs HBTs by transferring the epitaxial layers to high-thermal-conductivity substrates," *Electron. Lett.*, vol. 29, no. 21, pp. 1890–1891, Oct. 1993.

[3] B. Bayraktaroglu, J. Barrette, L. Kehias, C. I. Huang, R. Fitch, R. Neidhard, and R. Scherer, "Very high-power-density CW operation of GaAs/AlGaAs microwave heterojunction bipolar transistors," *IEEE Electron Dev. Lett.*, vol. 14, no. 10, pp. 493–495, Oct. 1993.

[4] W. Liu and A. Khatibzadeh, "The collapse of current gain in multi-finger heterojunction bipolar transistors: Its substrate temperature dependence, instability criteria, and modeling," *IEEE Trans. Electron Dev.*, vol. 41, no. 10, pp. 1698–1707, Oct. 1994.

[5] Y. Amamiya, C.-W. Kim, N. Goto, S. Tanaka, N. Furuhata, H. Shimawaki, and K. Honjo, "Microwave/millimeter-wave power HBTs with regrown extrinsic base layers," in *1994 IEEE Int. Electron Devices Meet. Dig.*, 1994, pp. 199–202.